

1. Specification

- Output signal spec.

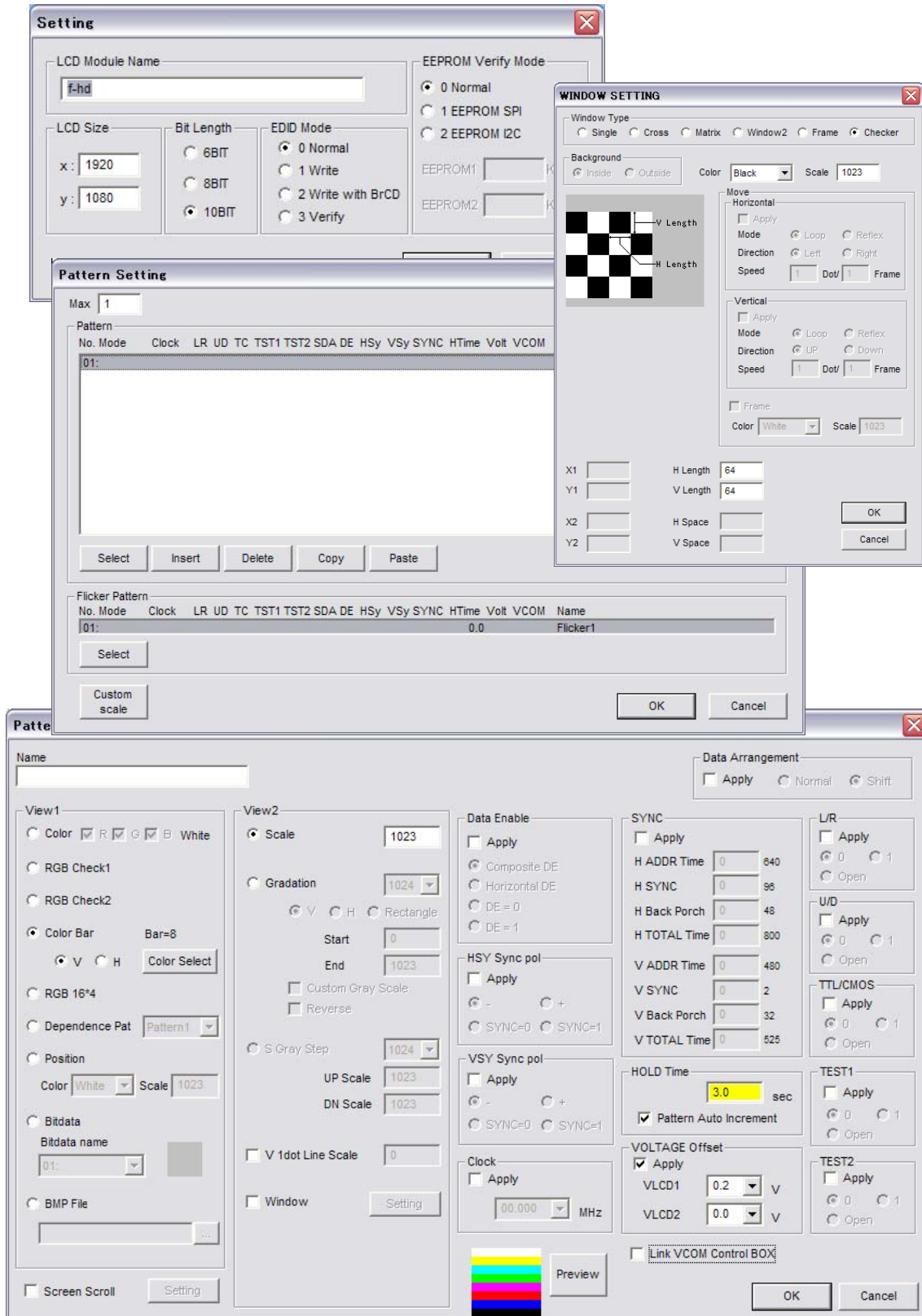
No.	項目	仕様
1	Dot Clock Frequency	Single Clock 100KHz ~ 135.0MHz Dual Clock 200KHz ~ 270.0MHz Quad Clock 400KHz ~ 300.0MHz Transmitter IC の性能により制約されます。
2	Frame Frequency	60Hz(標準) / 120Hz(倍速)
3	Resolution	WXGA 1280 × 786 WXGA 1280 × 800 WXGA 1366 × 768 F-HD 1920 × 1080 Max. 2048 × 2048
4	Output RGB Signal	10Bit LVDS Output
5	制御信号可変範囲	水平同期幅 2 ~ 2048 Dot Clock 水平ブランク幅 2 ~ 2048 Dot Clock 水平表示周期 2 ~ 2048 Dot Clock 水平周期 4 ~ 4096 Dot Clock 垂直同期幅 1 ~ 2048 Line 垂直ブランク幅 1 ~ 2048 Line 垂直表示周期 1 ~ 2048 Line 垂直周期 2 ~ 4096 Line
6	出力制御信号	Dot Clock / HD / VD / DE(ch1/ch2)
7	表示 Pattern Data	塗りつぶし等の標準 Pattern 縦 / 横 方向の階調(2/4/8/16/32/64/128/256) 縦 / 横 方向の特殊階調(2/4/8/16/32/64/128/256) 縦 / 横 方向の Color Bar RGB Checker / 1dot Checker / Flicker Window(Single / Cross / Matrix / Frame)

No.	項目	仕様
8	32Dots x 32Dots(繰り返し Pat.)	Full color 対応
9	8bit color bitmap	Full color 対応 最大 2048 x 2048 の自然画表示可能
10	I ² C EEPROM Read/Write (option)	EDID 対応 LCD Module に内蔵の PnP 用 EEPROM の Read/Write に対応
11	Auto gradation up/down	垂直同期信号に同期して 1 ~ 16 Frame 単位で増減 可能
12	Dot Clock Delay Line	CMOS Interface 使用時にハーネスの影響を吸収する 為、Dot Clock を data に対して位相調整が可能
13	LCD Module 設定数	400 機種(CF Card 容量に依存)

- Output voltage spec.

No.	項目	仕様
1	出力電圧(0.1V Step 設定可)	VLCD1 2.5V ~ 14.0V
		VLCD2 2.5V ~ 14.0V
2	出力電流	VLCD1 5A(Max)
		VLCD2 5A(Max)
3	ON Sequence	VLCD1 1 ~ 2000(ms)
		VLCD2 1 ~ 2000(ms)
		Signal 1 ~ 2000(ms)
4	OFF Sequence	VLCD1 1 ~ 2000(ms)
		VLCD2 1 ~ 2000(ms)
		Signal 1 ~ 2000(ms)

- Pattern Setting



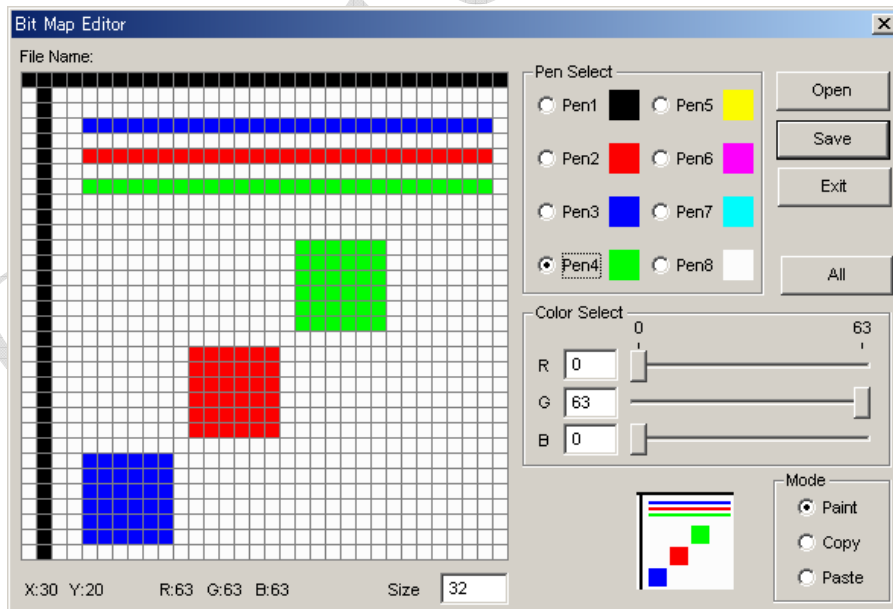
The image displays three overlapping dialog boxes from a software application:

- Setting Dialog:**
 - LCD Module Name: f-hd
 - LCD Size: x: 1920, y: 1080
 - Bit Length: 10BIT (selected)
 - EDID Mode: 0 Normal (selected)
 - EEPROM Verify Mode: 0 Normal (selected)
 - EEPROM1 and EEPROM2 fields are present.
- Pattern Setting Dialog:**
 - Max: 1
 - Pattern table with columns: No, Mode, Clock, LR, UD, TC, TST1, TST2, SDA, DE, HSY, VSY, SYNC, HTime, Volt, VCOM. Row 01: 0.0, Flicker1.
 - Flicker Pattern table with columns: No, Mode, Clock, LR, UD, TC, TST1, TST2, SDA, DE, HSY, VSY, SYNC, HTime, Volt, VCOM, Name. Row 01: 0.0, Flicker1.
 - Buttons: Select, Insert, Delete, Copy, Paste, Custom scale, OK, Cancel.
- WINDOW SETTING Dialog:**
 - Window Type: Checker (selected)
 - Background: Inside (selected), Color: Black, Scale: 1023
 - Move Horizontal: Apply (unchecked), Mode: Loop (selected), Direction: Left (selected), Speed: 1 Dot / 1 Frame
 - Move Vertical: Apply (unchecked), Mode: Loop (selected), Direction: UP (selected), Speed: 1 Dot / 1 Frame
 - Color: White, Scale: 1023
 - Dimensions: X1, Y1, X2, Y2, H Length: 64, V Length: 64, H Space, V Space
 - Buttons: OK, Cancel
- Patte Dialog (partially visible):**
 - Name: [empty]
 - Data Arrangement: Apply (selected)
 - View1: Color Bar (selected), Bar=8, Color Select, Scale: 1023
 - View2: Scale: 1023, Gradation: 1024, Start: 0, End: 1023, S Gray Step: 1024, UP Scale: 1023, DN Scale: 1023, V 1dot Line Scale: 0, Window: Setting
 - Data Enable: Apply (unchecked), Composite DE, Horizontal DE, DE=0, DE=1
 - HSY Sync pol: Apply (unchecked), SYNC=0, SYNC=1
 - VSY Sync pol: Apply (unchecked), SYNC=0, SYNC=1
 - Clock: Apply (unchecked), 00.000 MHz
 - SYNC: Apply (unchecked), H ADDR Time: 0/640, H SYNC: 0/96, H Back Porch: 0/48, H TOTAL Time: 0/800, V ADDR Time: 0/480, V SYNC: 0/2, V Back Porch: 0/32, V TOTAL Time: 0/525
 - HOLD Time: 3.0 sec, Pattern Auto Increment (checked)
 - VOLTAGE Offset: Apply (checked), VLCD1: 0.2 V, VLCD2: 0.0 V
 - Link VCOM Control BOX (unchecked)
 - Buttons: OK, Cancel

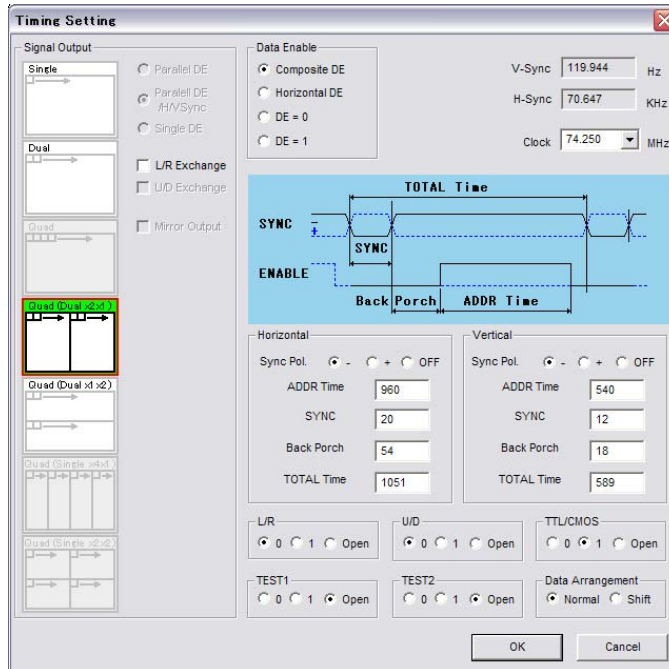
- Preview Window



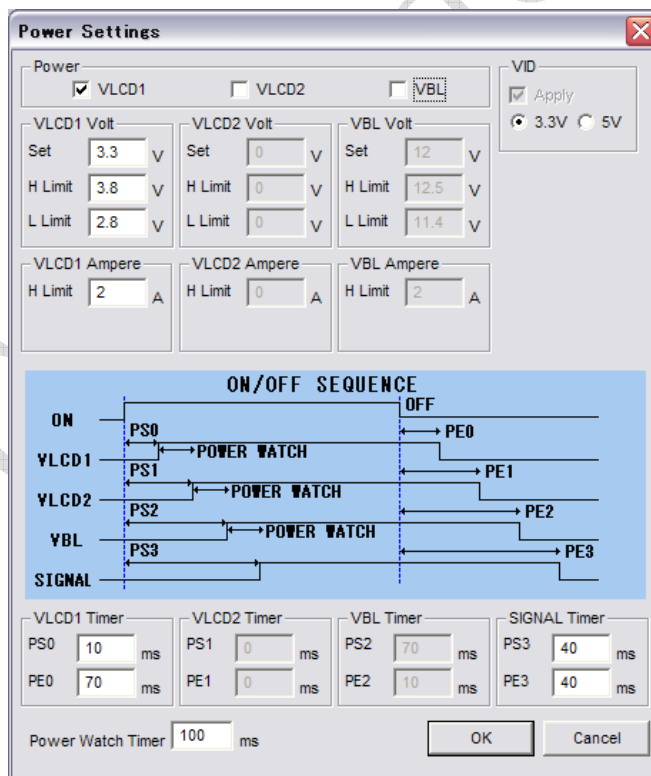
- BITMAP Editor



- Timing Setting



- Power Setting



(注) 装置には VBL は搭載致しません。